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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,024	11/16/2000	Masato Mitsuhashi	108066-00018	3168

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,024	MITSUHASHI ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/8/03 and 11/6/00* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on ____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the amended claim 5's counting means for "counting a number of the PLL clock signal" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended claims 5 recites "counting a number of the PLL clock signal". Neither the Specification nor the drawing as originally presented supports this limitation.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for constructing the clock switching circuit with the PLL circuit and flip-flop groups in the claimed structure, does not reasonably provide enablement for preventing the clock switching circuit from producing a hazard by the ratio between the numbers of the flip-flop groups. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The claim language merely states that the number of the second flip-flop group is greater

than the number of the first flip-flop group. It does not enable one on how much greater and what the number of the second flip-flop group has to be in order to prevent the so-called hazard.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Parmenter et al. (U.S. Patent No. 5,679,353).

Referring to claims 7-8: Parmenter discloses a PLL circuit (figure 2, structure 15) that generates a fast clock (figure 2, node 2X_CLK2) whose frequency is more than twice as much as a frequency of the basic signal (figure 2, node 17). Parmenter further discloses multiplexers and their associated control means (figure 2, structures 19, 21, and their control means structure SR1), which are equivalent to the claimed inhibiting circuit that inhibits said fast clock by a time (figure 2, the logic circuit node 27, column 2, lines 11-19) when said basic clock disappears in said output in the case of switching said output from said basic clock to the fast clock, or a term which depends on the difference between said frequency of the basic clock and the frequency of the fast clock in the case of switching. Hence, claims are anticipated by the Parmenter.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claim 5 is rejected under 35 U.S.C. 102(b) as being unpatentable over the Yokogawa et al. (U.S. Patent No. 4,872,155) in view of Ishikawa (U.S. Patent No. 6,346,830).

Referring to claim 5: Yokogawa's invention discloses a PLL circuit including a phase comparator comparing two asynchornized clocks' signals (column 4, lines 47-51), and it further discloses that the PLL generates the clock in synchronism (column 5, lines 4-5); thus, Yokogawa discloses the receiving a PLL clock signal generated from a PLL circuit based on the basic clock signal. Yokogawa further discloses the counting the clock signal number, inhibiting the clock output, and output PLL clock signal after a predetermined number of clock signals (column 4, lines 59-64, column 5, lines 4-6, figure 10). Although Yokogawa discloses the PLL circuit for comparing phases of different clocks' speeds (column 4, lines 47-49), Yokogawa does not explicitly disclose that the PLL clock is faster than the clock speed as the amended claim recites.

Ishikawa discloses an I/O interface with PLL circuits for supporting different I/O clock speeds (figure 5). Ishikawa teaches one to synchronize the clock speed in response to data output and data input with different PLL speeds (column 2, lines 53-67, column 3, lines 1-30). Ishikawa discloses that in order to have a reliable reception of data, it is necessary to establish the value of data at a particular phase of the clock (column 2, lines 29-32), and Ishikawa teaches applying the PLL to synchronize either a faster clock speed or a slower clock speed to establish the value of data at a particular phase of the clock (column 2, lines 53-67, column 3, lines 1-30). Since Ishikawa's interface is to connect two devices with two different speeds, and Ishikawa has two separate PLLs for transmitting data at two opposite directions, one of the Ishikawa's PLLs must be faster than the system/reference clock due to the different speeds between the two devices.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the Ishikawa's teaching onto Yokogawa because Ishikawa teaches one to establish a reliable data reception by establishing the value of data at a particular phase of the clock with two separate PLLs synchronizing both input data speed and output data speed.

Response to Arguments

9. In response to Applicant's argument that the claim 6 is rejected under 35 U.S.C. §112 first paragraph as a formal matter, and Applicant argues that the Specification as originally presented does support a full and clear disclosure to enable a person skilled in the art (Remark, page 2, last 2 paragraphs, page 3): As quoted by the Applicant that Specification page 13, lines 10-16 provides "The differences in number of stages is set according to the difference in

frequencies of the first clock X'tal and the second clock PLL. In the example shown in Fig. 5, the second flip-flop group 45 comprises 2N stages of flip-flops F/F (1a)(1b) to F/F(Na)(Nb)". The quoted Specification does not sufficiently provide information to enable one with skill in the art. The quoted statement merely states that the number is set according to the difference, but the quoted statement does not explain how the differences in frequency reflect or relate to the number of stages.

10. In response to Applicant's argument that Yokogawa does not show at least a PLL clock signal faster than the basic clock (Remark, page 5, lines 11-12): This argument is towards the newly submitted amendment; see the revised Office Action above.

11. In response to Applicant's argument that Yokogawa does not show "counting a number of PLL signal after inhibiting outputting the basic clock signal" (Remark, page 5, lines 12-13): Yokagawa discloses that the clock signal is passed through both the Gate Pulse Generator and Sync Detector, then to the PPL for outputting. Because Yokagawa's Gate Pulse Generator, Sync Detector, and the PPL control the clock output, these circuits are inhibits outputting the clock signals. The argument of "counting a number of PLL signal" is towards the newly submitted amendment; see the revised Office Action above.

12. In response to Applicant's argument that Parmenter's multiplexers are not equivalent to the claimed inhibiting circuit (Remark, page 7, lines 1-2): The claimed inhibiting circuit inhibits a first clock signals when switching to a second clock signals. Parmenter's multiplexers and the associated control means select the signals from either the CLK2 or the PLL output 2X_CLK2. Thus, Parmenter discloses inhibiting one clock signal while selecting another clock signal.

Allowable Subject Matter

13. Claims 1-4 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior arts on record do not disclose or explicitly teach the claimed structure.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's

PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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Justin King
February 20, 2005